Processor Verification – Twitter Chat
October 28, 2013 #SoC

Introduction

Transcript from Twitter Chat conducted at 12 Noon EST on October 28, 2013. Hash tag is #SoC.

Participants

@DevOps, @NielsEngelen, @erocksindia, @Teraptor, @muralibulusu, @vasanth_vaidya, @GopiBulusu

Twitter Transcript

The Twitter chat was hosted by @vasanth_vaidya with @GopiBulusu as the main guest.

Vasanth Vaidyanathan @vasanth_vaidya All questions are denoted by Qn and corresponding answers are indicated by An #soc @GopiBulusu
Vasanth Vaidyanathan @vasanth_vaidya @GopiBulusu Q1: What is an #SoC? #processor #verification #agile Gopi Bulusu @GopiBulusu @vasanth_vaidya A1: A system on chip or an #SoC is a very large scale integrated circuit chip that contains all functions of a system #SoC
Vasanth Vaidyanathan @vasanth_vaidya @GopiBulusu Now, let us go to Q2: What is #ASDM #SoC Would you be able to explain this? Gopi Bulusu @GopiBulusu @teraptor a2: #ASDM brings twin benefits of agile development process and System Design Automation #SDA to #SoC development Gopi Bulusu @GopiBulusu @vasanth_vaidya a2: #SoC design starts with market demand for systems (consumer electronics) #Agile System Development with Models #ASDM
Vasanth Vaidyanathan @vasanth_vaidya @GopiBulusu Q3: Why are #MAS skills important ? #SoC #agile #processor #sda #eda #system #design

#embedded #ASDM

Gopi Bulusu @GopiBulusu
A3|: #MAS or Modelling Abstraction and Synthesis skills are essential for developing complex systems in general and #SoC with #SDA and #ASDM

Vasanth Vaidyanathan @vasanth_vaidya
@GopiBulusu Q4: Curious, how is SoC different from a Processor #SoC ? Could you explain? #agile #processor #verification #design #eda #sda

Gopi Bulusu @GopiBulusu
A4: An #SoC may include application, audio, video processors - communication peripherals, memory subsystem in a network #NoC

Vasanth Vaidyanathan @vasanth_vaidya
@GopiBulusu Q5: What is the challenge in verifying a processor? #SoC #ProcessorVerification #agile #ASDM #MAS #eda #sdaVasanth Vaidyanathan @vasanth_vaidya

Gopi Bulusu @GopiBulusu
A5: A 5-stage pipeline 32 bit processor can take 2 ^ 32 ^ 5 different inputs and states a very large number to test ! #SoC #SDA #ASDM

Vasanth Vaidyanathan @vasanth_vaidya
@GopiBulusu Q6: How does constrained random testing help #SoC #ProcessorVerification #agile #sda #eda #design

Gopi Bulusu @GopiBulusu
A6: constraints allow the overall test space to be brought down to manageable size, randomness gives uniformity in test space coverage #SoC

Vasanth Vaidyanathan @vasanth_vaidya
@GopiBulusu Q7: What is Test Synthesis #SoC #ProcessorVerification #design #eda @sda #embedded #asdm #modeling

Gopi Bulusu @GopiBulusu
A7: an #SMDL processor model can be used to synthesise tests and results using Teraptor Explorer for processor verification #SoC

Vasanth Vaidyanathan @vasanth_vaidya
@GopiBulusu Q8: How do I learn more about #ProcessorVerification? #SoC #agile #embedded #sda #eda
Gopi Bulusu @GopiBulusu

@A8: Checkout http://www.sankhya.com/info/products/teraptor/verify.html#page=page-7 … ; or attend an

upcoming #ASDM event http://www.hamara.in/asdm_tutorial/oct2013/index.html … #SoC #ProcessorVerification
Vasanth Vaidyanathan @vasanth_vaidya @GopiBulusu Super! Thank you so much for taking the time to chat. #SoC #agile #embedded #system #design #processor #verification Gopi Bulusu @GopiBulusu @vasanth_vaidya @teraptor it was cool, thanks for hosting - look forward to future #SoC chats

For more information

Contact support@sankhya.com for more information.

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